Abstract

A delay lock circuit includes a measuring path, a forward path, and a feedback path. The measuring path samples a pulse with a reference signal in a measurement to obtain a measured delay. The forward path delays the reference signal based on the measured delay to generate an internal signal. The feedback path includes a calibrating unit for generating the pulse based on a plurality of feedback signals generated from the reference signal. The delay lock circuit further includes a monitoring unit for monitoring the measurement. Based on the monitoring, the monitoring unit enables the calibrating unit to conditionally adjust the width of the pulse.